

REMARKS

The Applicant has filed the present Response in reply to the outstanding Official Action of February 10, 2004, and the Applicant believes the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

In the outstanding Official Action, the Examiner rejected Claims 1-4 pursuant to 35 U.S.C. §102(b), as being allegedly anticipated by Jaber et al. (U.S. Patent No. 5,614,838) (hereinafter "Jaber"). Specifically, regarding Claim 1, the Examiner asserted that Jaber discloses an apparatus and method for performing level sensitive scan design (LSSD) testing of the integrated circuit device under test wherein the integrated circuit device contains the claimed elements.

We respectfully disagree with the Examiner's assertions and traverse the rejection for at least the following reasoning.

Claim 1 is directed to, inter alia, an integrated circuit device for being put to a delay test using a scan path test circuit for scan path testing comprising a two pulse generator for generating two pulses spaced from each other by a period equal to the test clock. The two pulses generated by the two pulse generator is then supplied to the scan path test circuit.

Jaber does not disclose or suggest a two-pulse generator for generating a two pulse signal for scan path testing.

Insofar as rejections pursuant to 35 U.S.C. § 102(e) are concerned, it is axiomatic that anticipation pursuant to §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of

the claim and the disclosure of the applied prior art reference. Stated another way, the prior art reference must contain within its four corners adequate direction to practice the invention as claimed. A corollary to the aforementioned rule, which is equally applicable, states that the absence from the applied prior art reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571 (Fed. Cir. 1986).

In the present invention, the two-pulse generator extracts two pulses from the test clock in timed relation to a control pulse and supplies the extracted two pulses to a scan path test circuit. The Examiner contends that the two-generator is element 200 of Jaber and the two pulse signal is CLKG 205. This contention is incorrect. CLKG 205 disclosed in Jaber is a high speed system clock. This system clock is generated by an on-chip clock and phase lock loop circuit 204. In contrast, the two-pulse signal of the present invention is generated by the test clock, which is not necessarily an on-chip clock. CLKG 205 is not generated by COP_CLKG 211 which is the test clock.

Furthermore, the purpose of Jaber is to reduce the power dissipated in the electronic components during testing. See col 3, lines 35-40 (test control logic for controlling application of the high speed clock signal to circuits on the high speed component to cut off the high speed clock during one phase of the multiphase test). The reference further teaches that in the preferred embodiment to greatly reduce the power dissipation in the test phase, the high speed clock CLKG is stopped during the scan phase of the test. Therefore, this would teach away from supplying the CLKG clock signal, which the Examiner contends is the two-pulse signal, to a scan path testing circuit, since according to Jaber, the clock is stopped during scan phase of testing.

In addition, Fig. 5 depicts the CLKG signal as having more than two-pulse lengths, whereas, the claimed two-pulse generator only extracts *two-pulses* from the test clock. (*Emphasis added*)

Lastly, the purpose of the prior art reference is completely different from the claimed invention. The present invention uses a two-pulse signal for enabling path delay testing between scan flip-flops whereas Jaber is concerned with power dissipated during circuit testing and thus stops the high speed clock during testing.

Accordingly, Jaber fails to teach or suggest all of the claim limitations of Claim 1, as the reference fails to disclose the two-pulse generator for generating two-pulses, and that the generated two-pulses are supplied to the scan path test circuit.

In the Official Action, the Examiner also rejected Claims 21-24, 30 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Jaber. The Examiner stated that Jaber does not explicitly disclose a test board on which an integrated circuit device is removably mounted and a clock generator mounted on the test board for outputting a test clock, however the Examiner noted that test boards are well known. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Jaber and with a known test board to arrive at the claimed invention.

We respectfully disagree with the Examiner's rejection of Claims 21-24, 30 and 32 and traverse for the same reasoning as identified above. Jaber fails to teach the semiconductor integrated circuit device according to Claim 1. Accordingly, since Jaber fails to teach or suggest all of the limitations of Claim 21-24, 30 and 32, the Applicant submits that the claims are patentably distinct.

For all the foregoing reasons, the Applicant respectfully requests the Examiner to withdraw the rejections of independent Claim 1 pursuant to 35 U.S.C. §102(b). Furthermore, the Applicant respectfully requests the Examiner to withdraw rejections of dependent Claims 2-4 based at least on their respective dependencies, whether direct or indirect, from independent Claim 1. Applicant also respectfully requests the Examiner to withdraw the rejections of independent Claims 21-24 and dependent Claims 30 and 32 pursuant to 35 U.S.C. § 103(a).

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Seth Wenfeld", is written over the printed name.

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